Abstract

[0033] An apparatus and a method for rapidly flushing a cache memory device, including a list structure to track changes in a cache, which may be implemented on the processor die separate from the cache memory. The list structure allows for access to a relatively small store of data to determine whether or not a cache entry needs to be written to the main memory. Choosing the format of the list structure, allows one to make tradeoffs between area needed on a chip and the amount of efficiency in the cache flushing process.